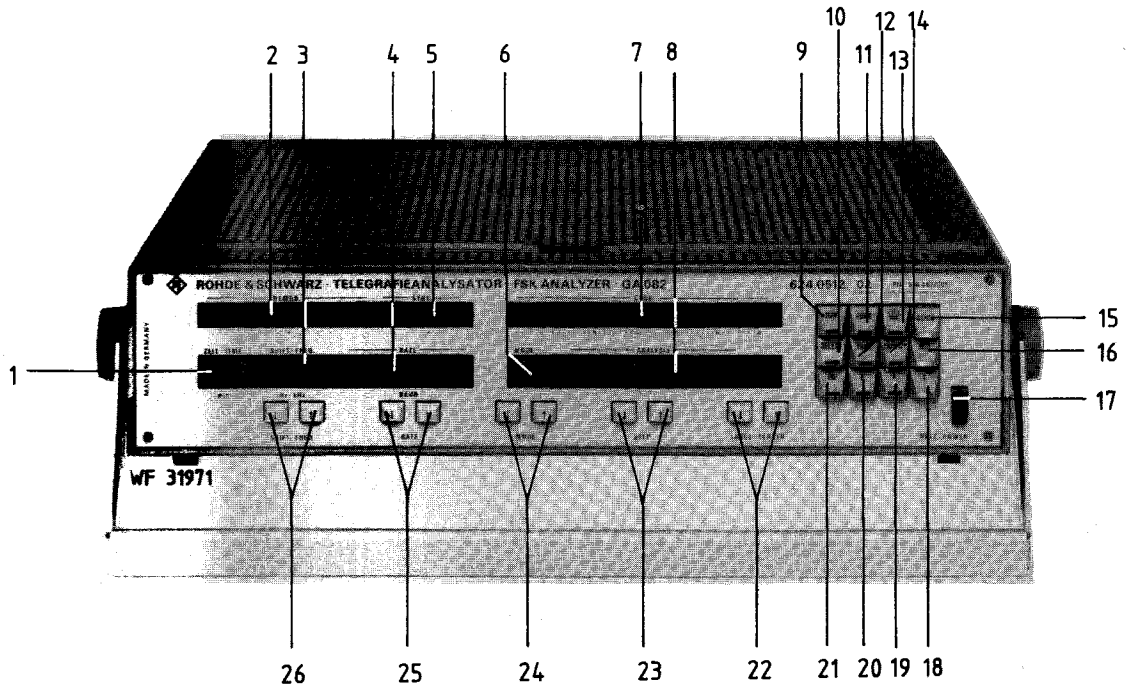


Bild 2-1 Frontansicht

Fig. 2-1 Front view

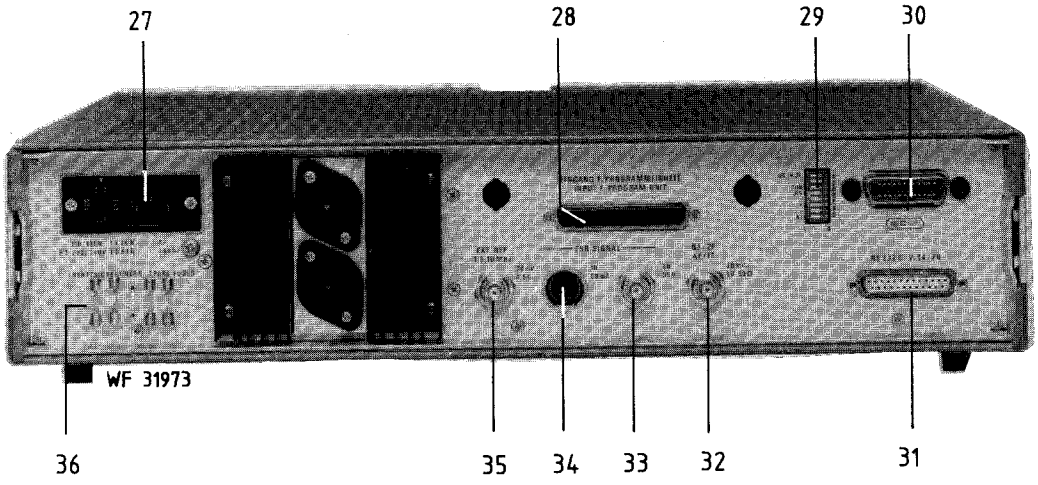


Bild 2-2 Rückansicht
Fig. 2-2 Rear view

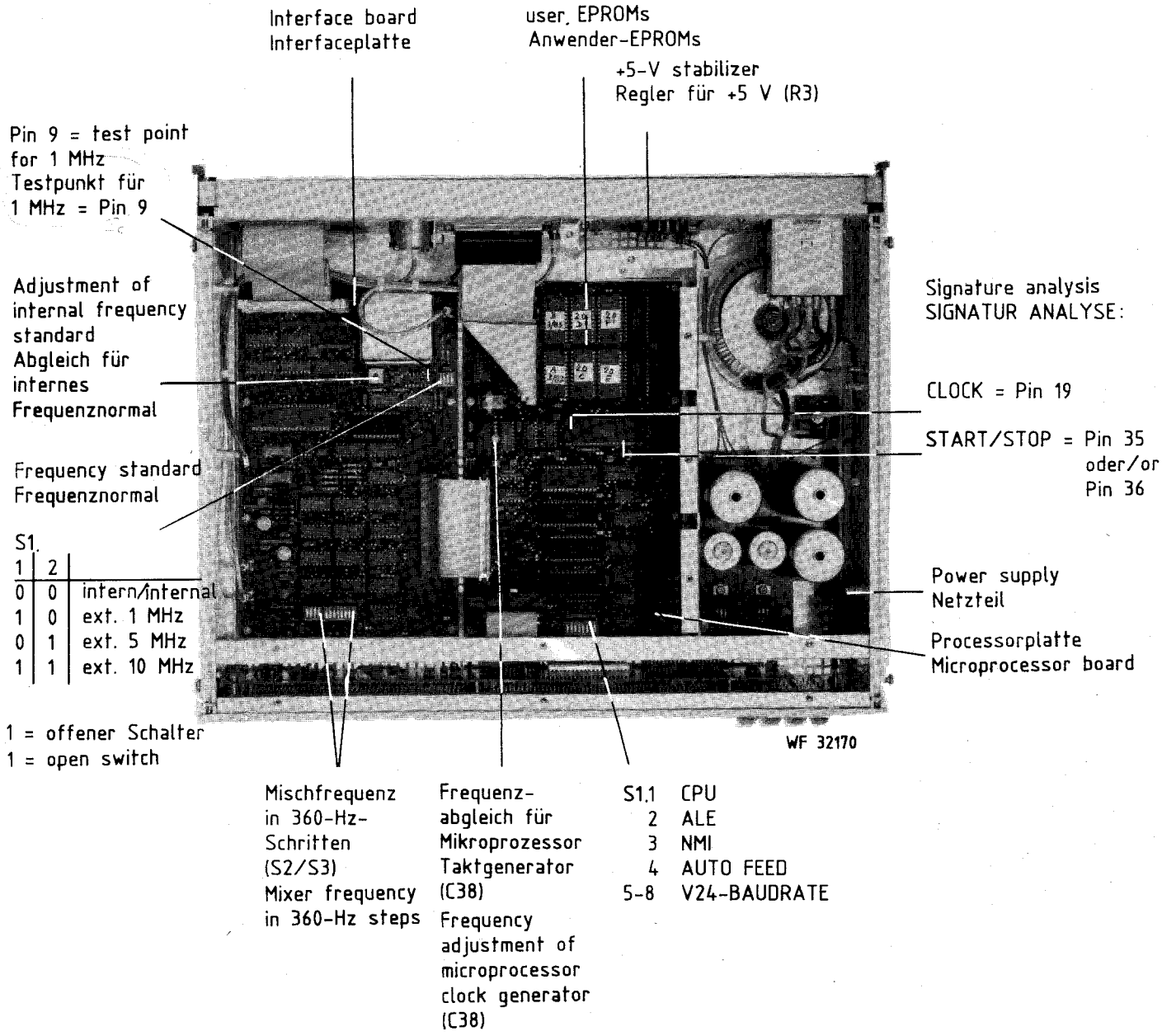


Bild 2-5 Lage der internen Wahlschalter und Trimmer

Fig. 2-5 Location of internal selector switches and trimmers

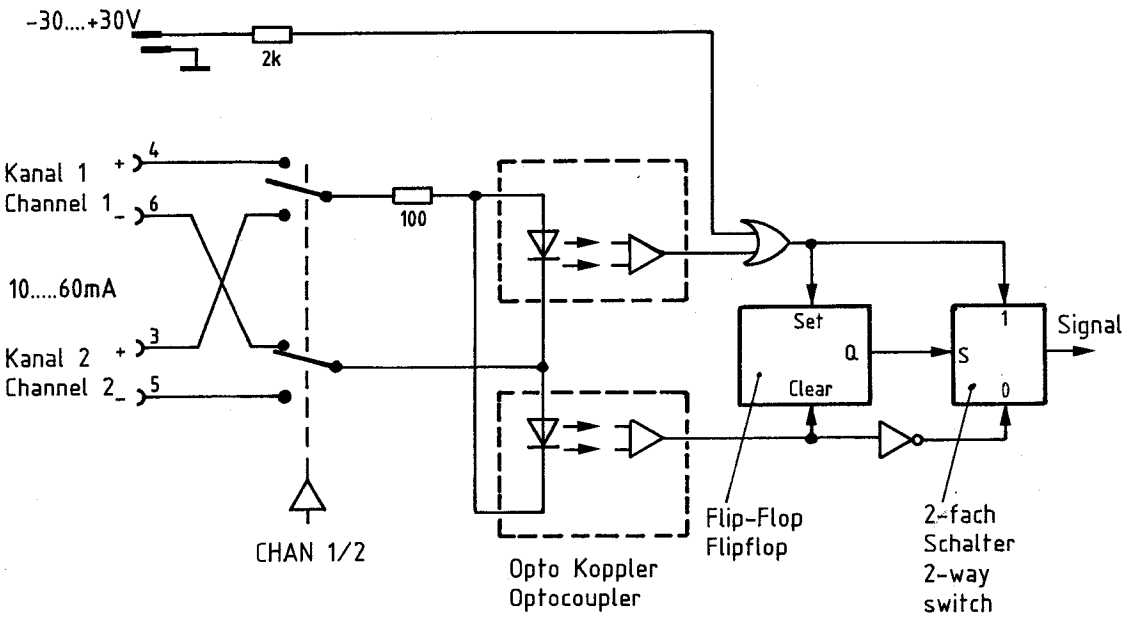


Bild 2-4 Eingangsschaltung für demoduliertes Signal

Fig. 2-4 Input circuit for demodulated signal

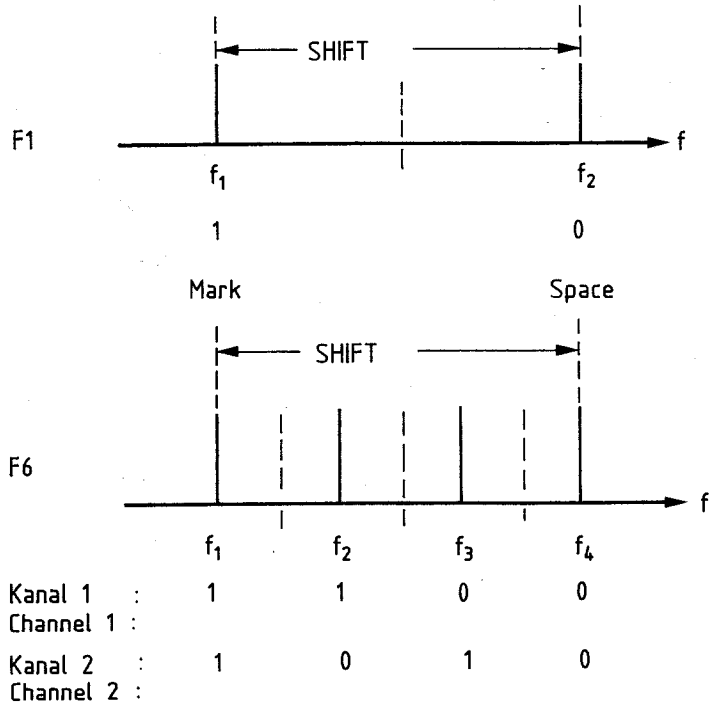


Bild 2-5 F1- und F6-Modulation

Fig. 2-5 F1 and F6 modulation

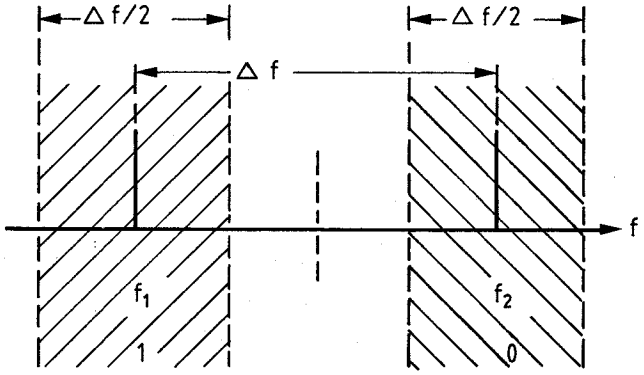


Bild 2-6 Frequenzbereiche bei F1-Demodulation

Fig. 2-6 Frequency ranges with F1 demodulation

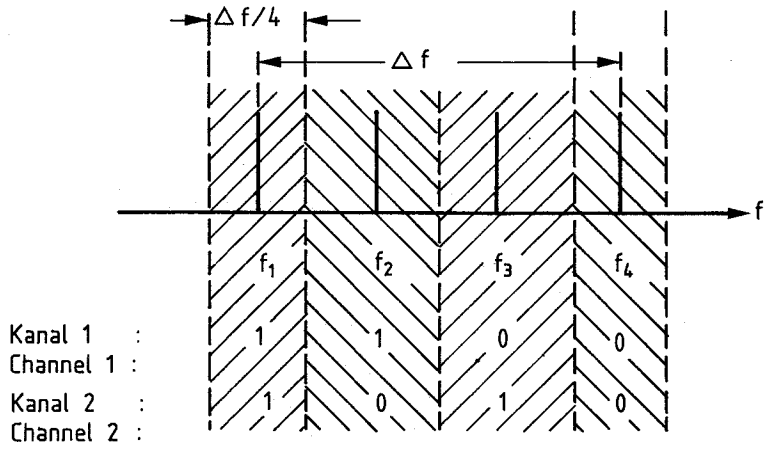


Bild 2-7 Frequenzbereiche bei F6-Demodulation

Fig. 2-7 Frequency ranges with F6 demodulation

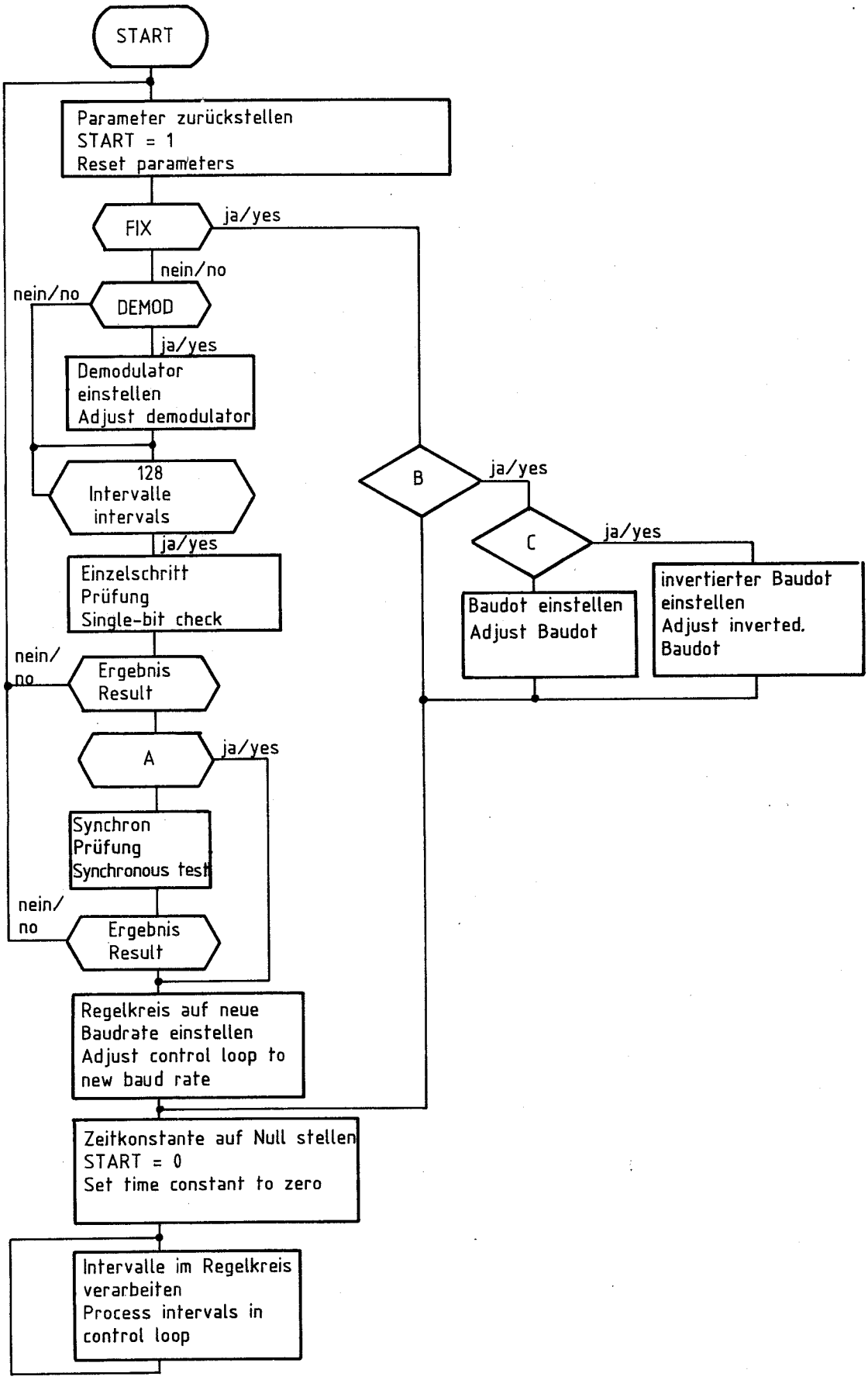


Bild 2-8 Programmablauf nach START

Fig. 2-8 Program sequence after START

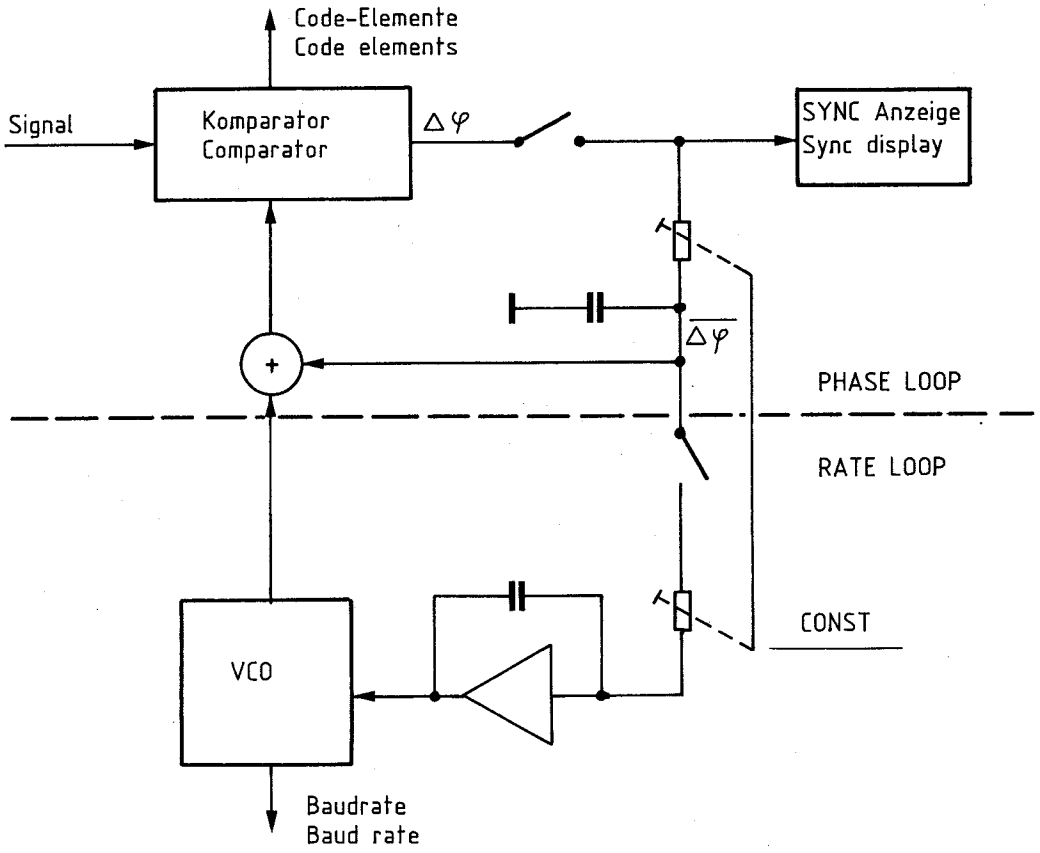


Bild 2-9 Schema des Regelkreises

Fig. 2-9 Diagram of control loop

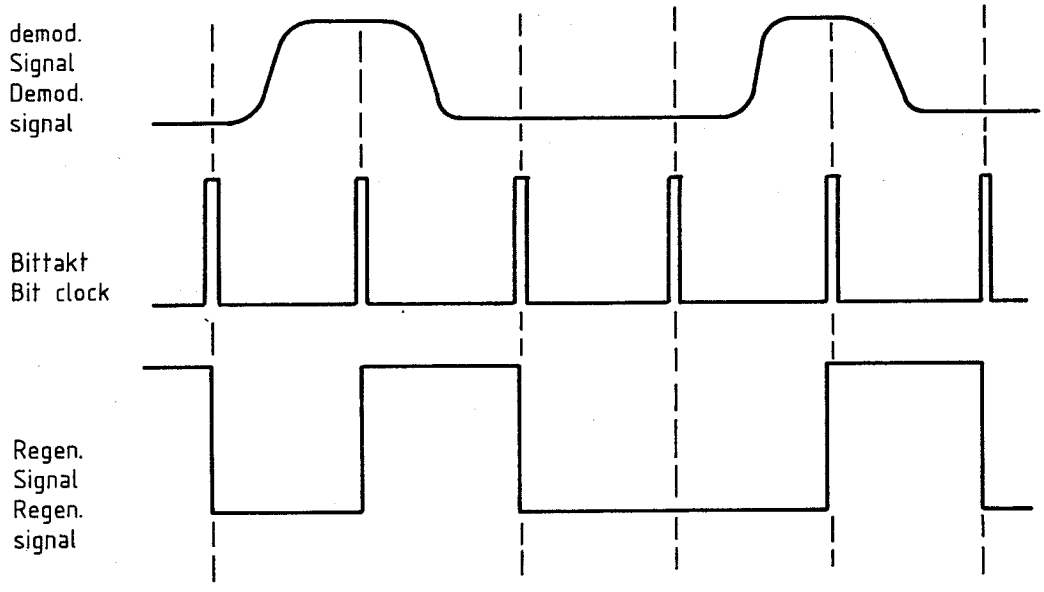


Bild 2-10 Bittakt und regeneriertes Signal

Fig. 2-10 Bit clock and regenerated signal

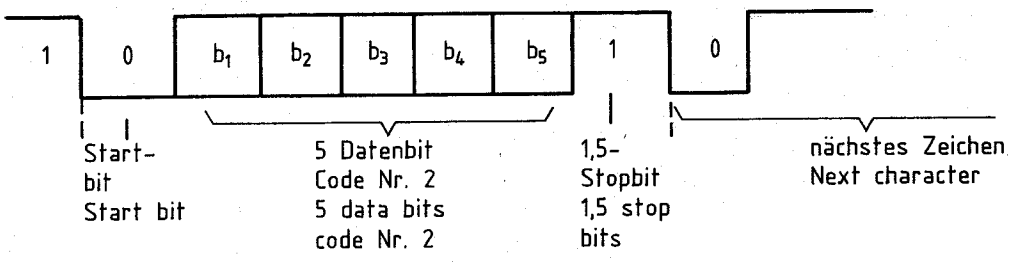


Bild 2-11 Baudot-Code

Fig. 2-11 Baudot code

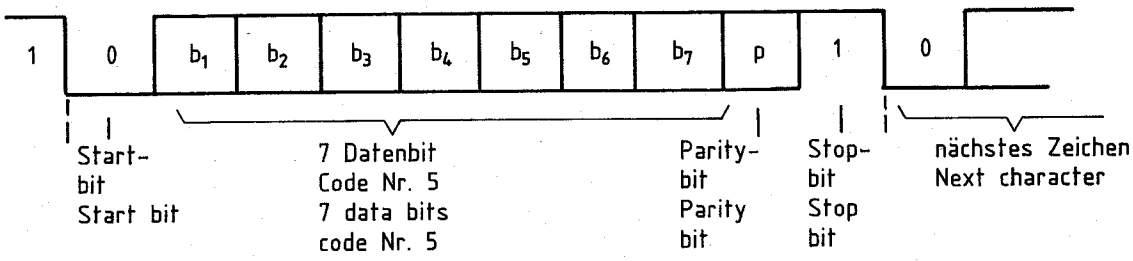


Bild 2-12 ASCII-Code-Zeichen

Fig. 2-12 ASCII code character

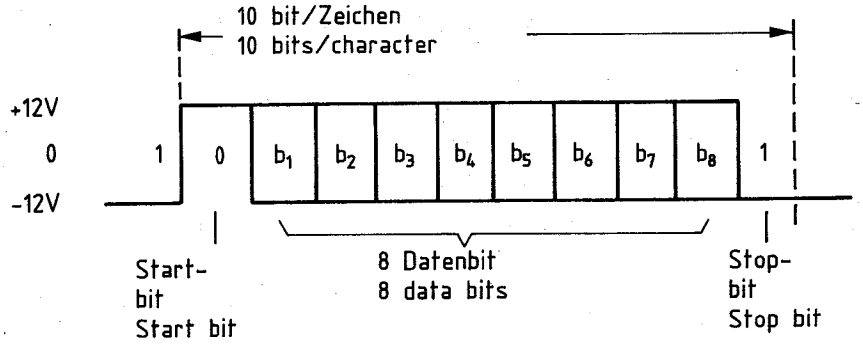


Bild 2-13 Zeichenformat für V.24-Schnittstelle

Fig. 2-13 Character format for V.24 interface

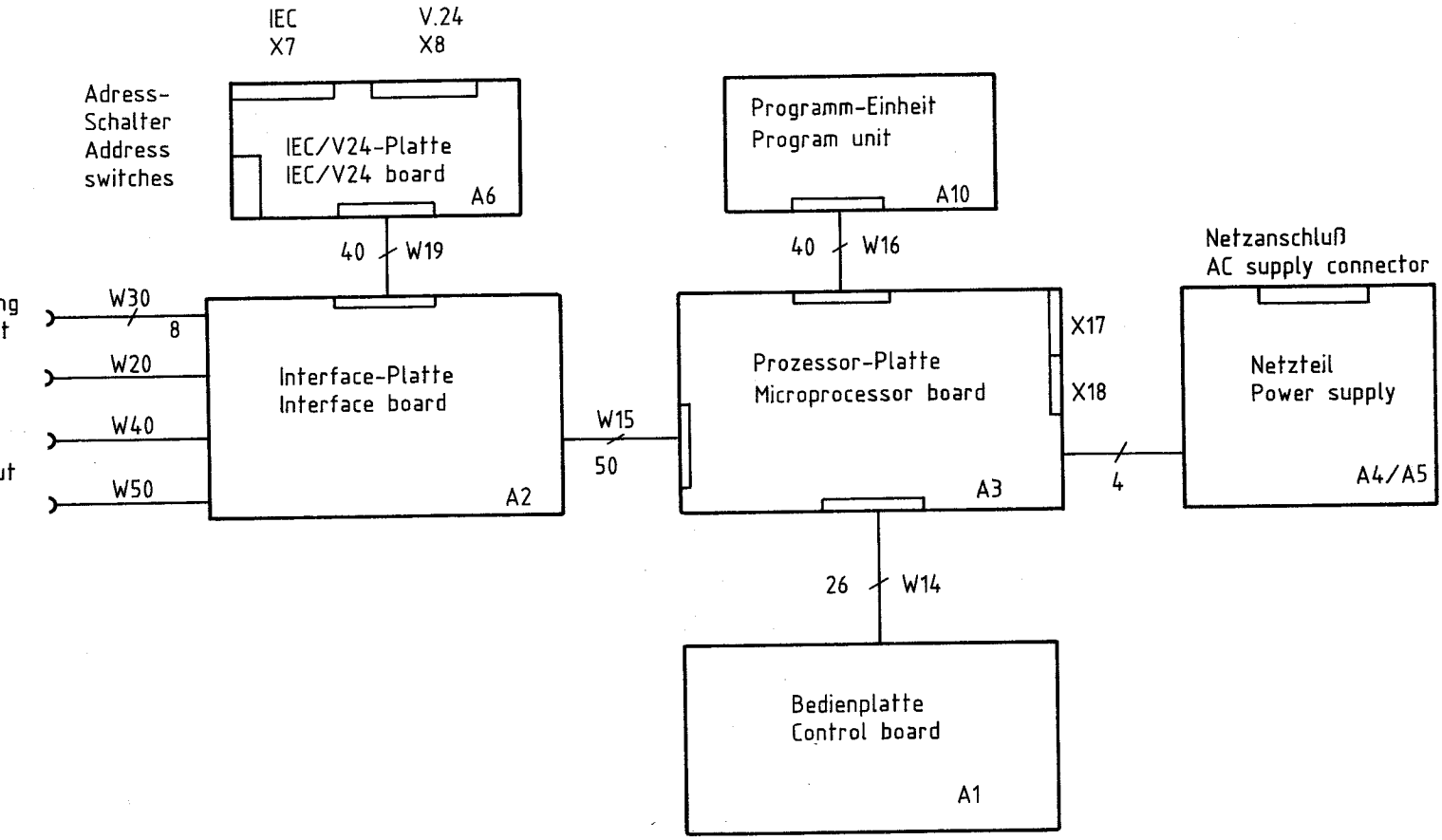


Bild 4-1 Teilsysteme des GA082

Fig. 4-1 Modules of GA082

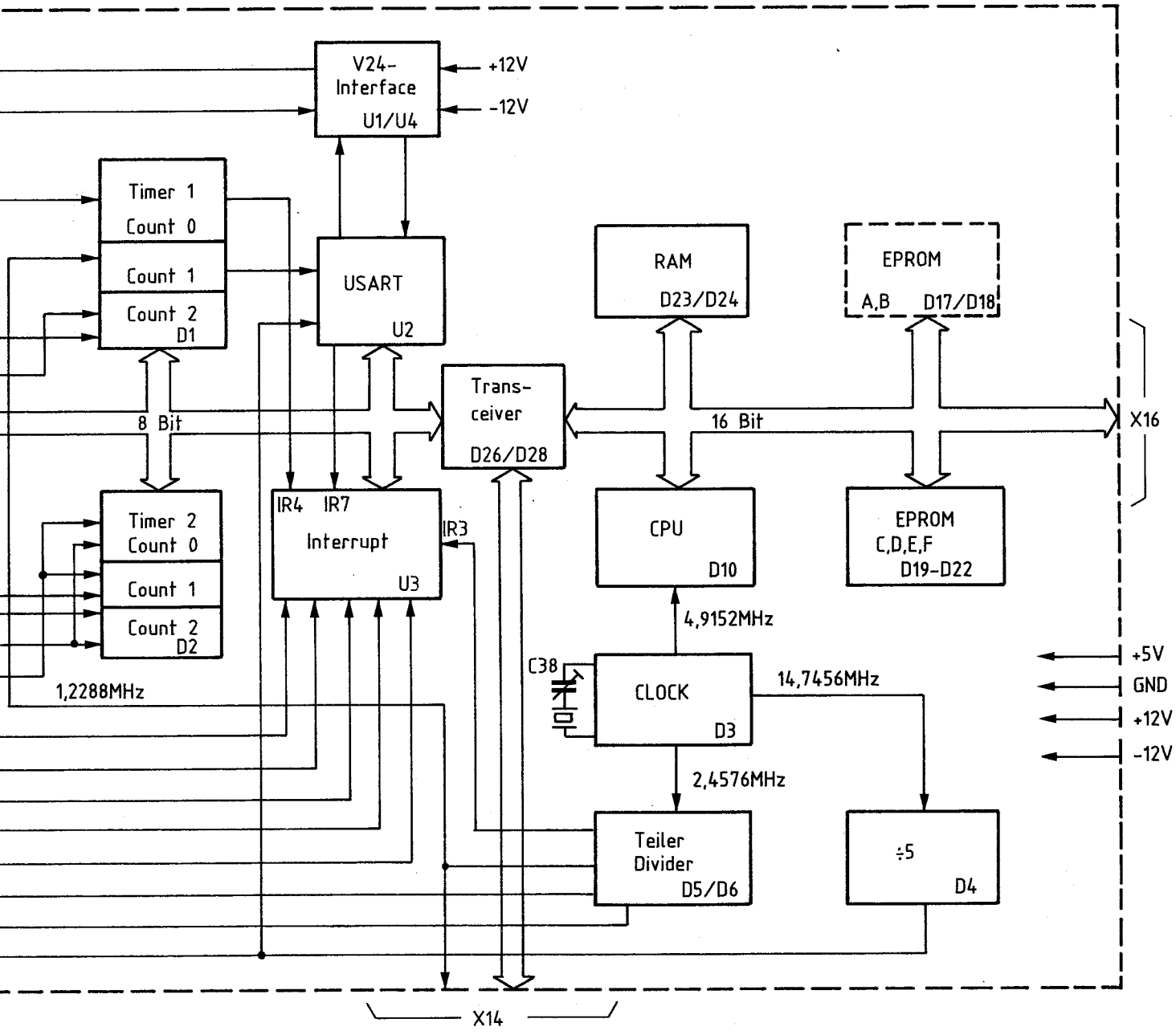


Bild 4-2 Blockschaltbild der Prozessorplatte

Fig. 4-2 Block diagram of microprocessor board

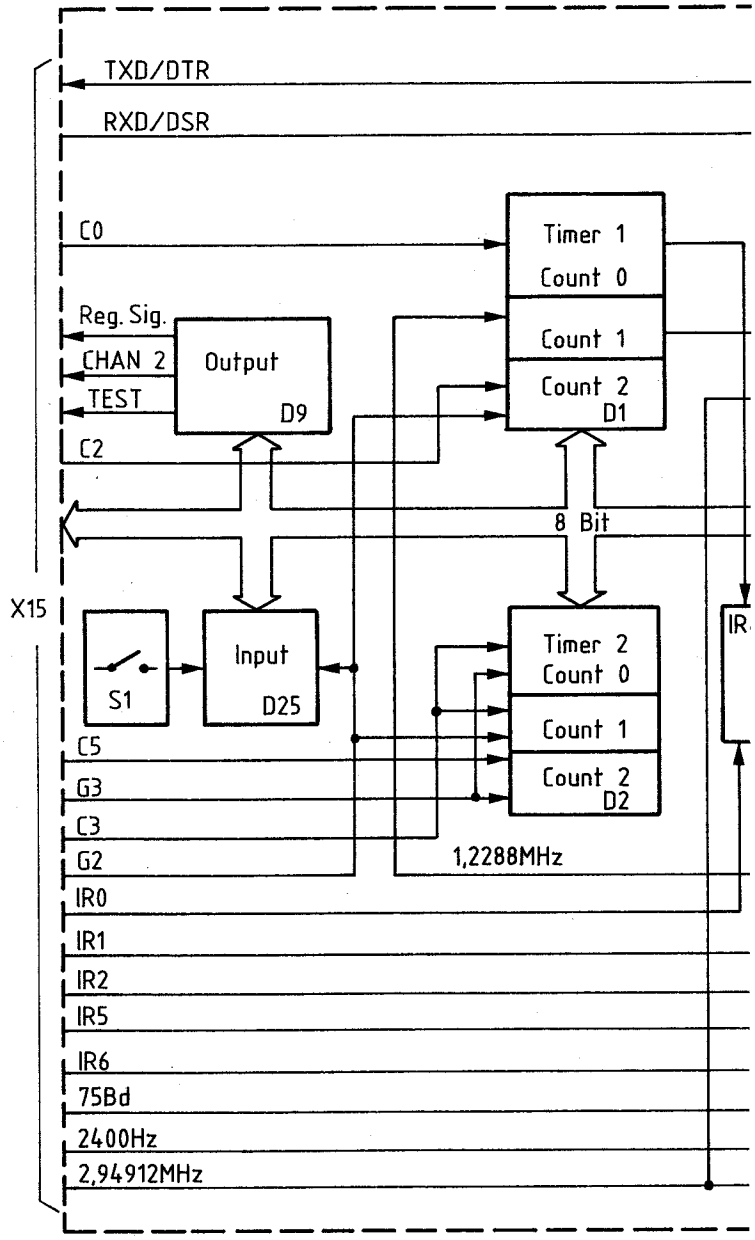


Bild 4-2 B

Fig. 4-2 E

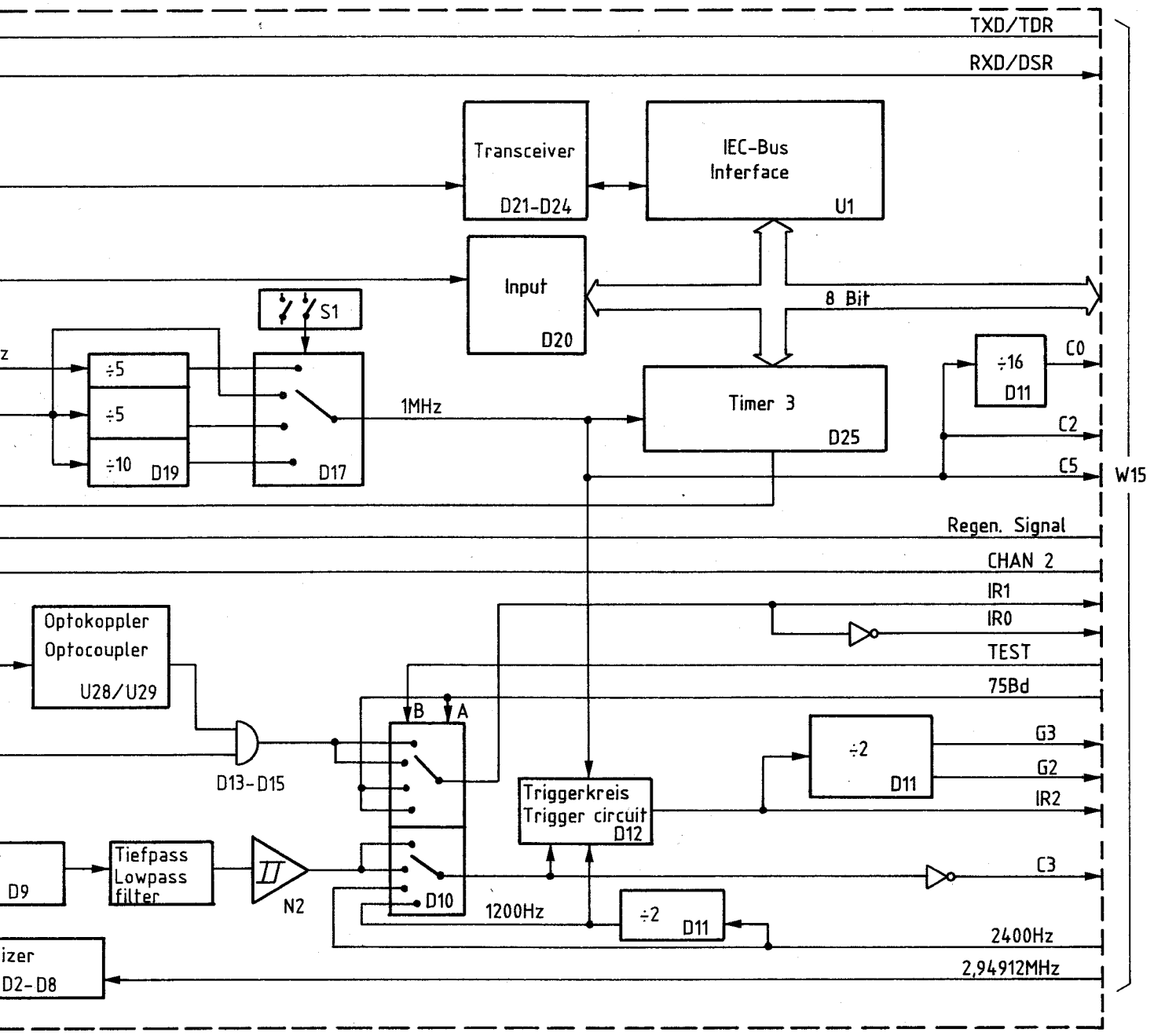


Bild 4-3 Blockschaltbild der Interface-Platte

Fig. 4-3 Block diagram of interface board

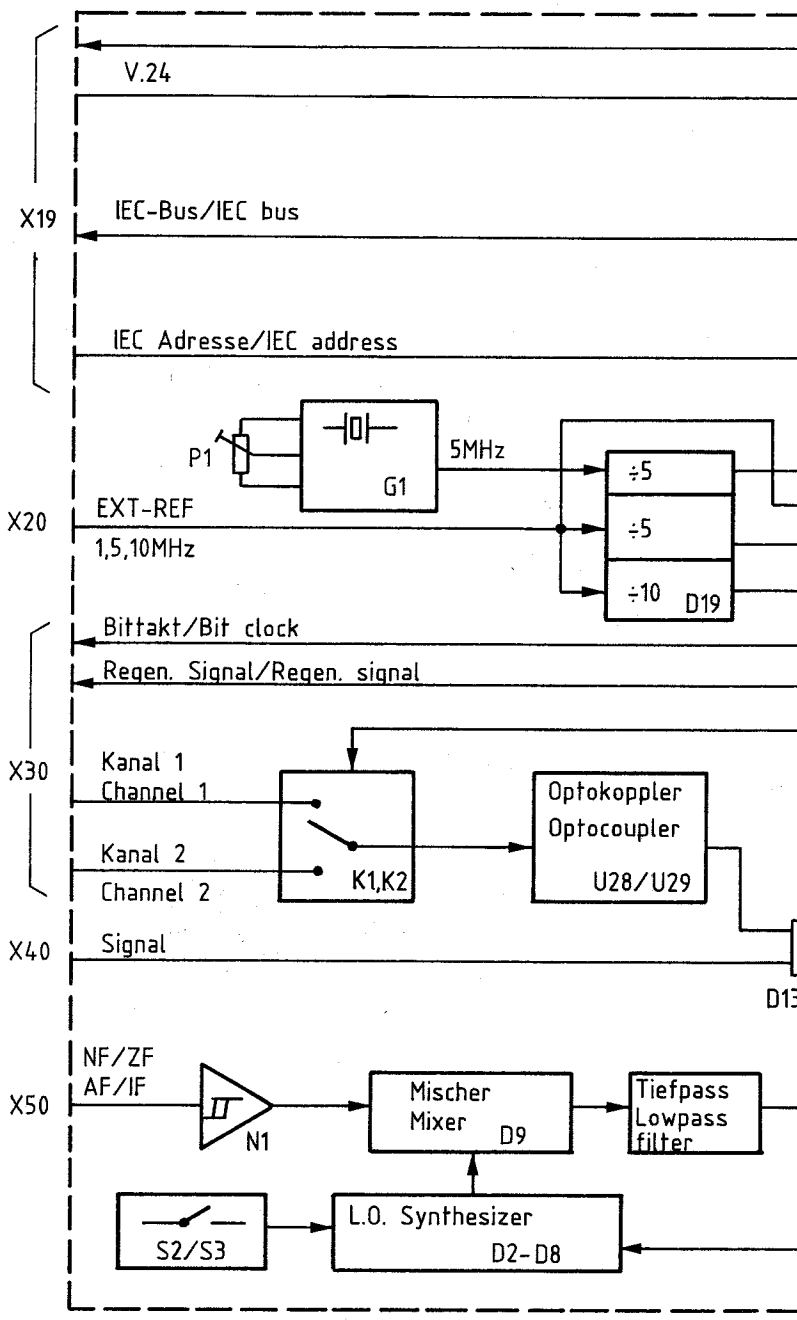


Bild 4-3

Fig. 4-3

GA082

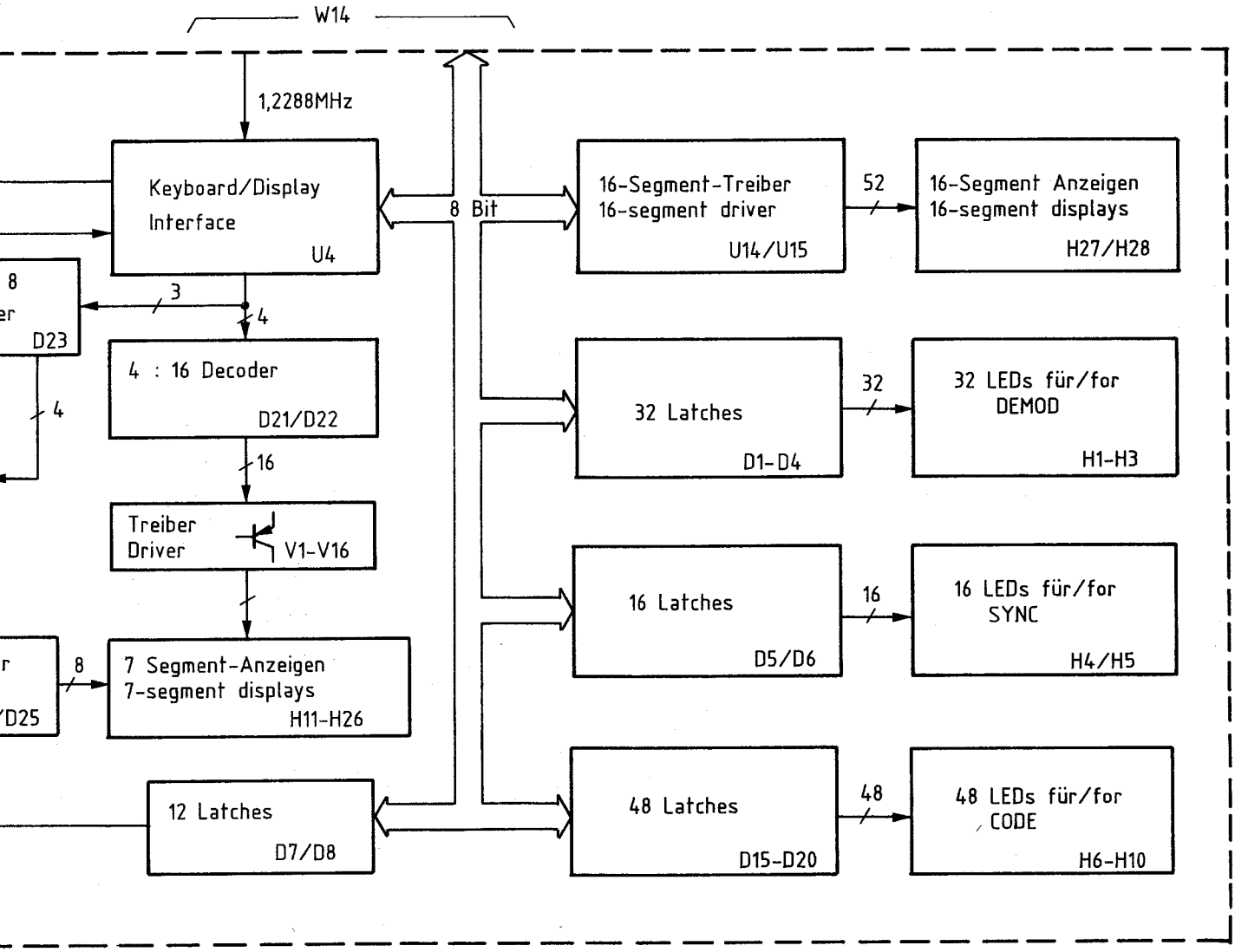
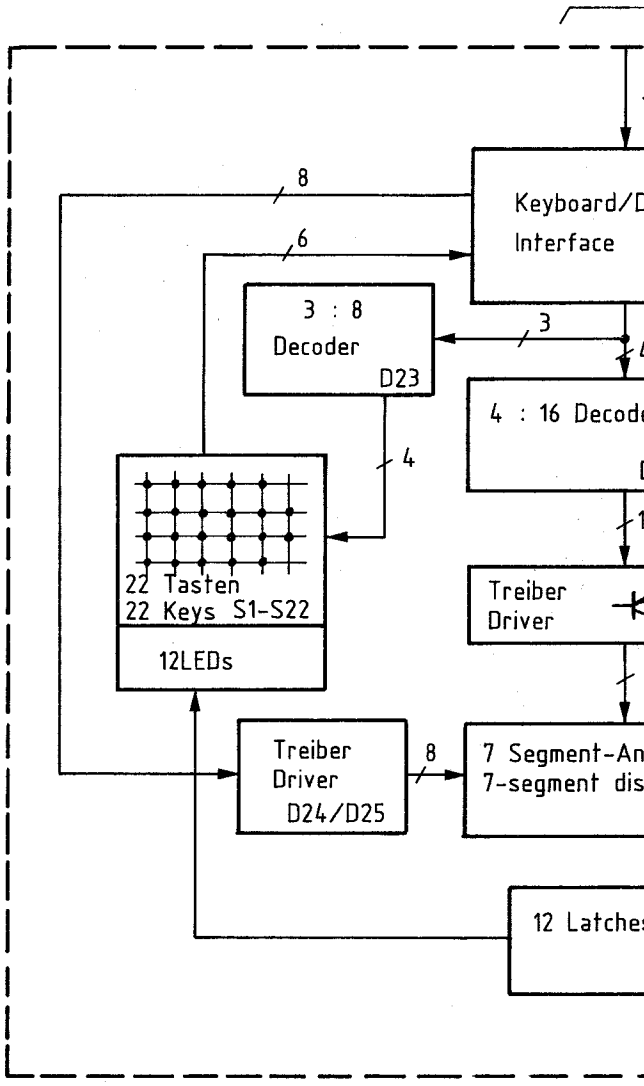


Bild 4-4 Blockschaltbild der Bedienplatte

Fig. 4-4 Block diagram of control panel


8
6
Keyboard/D
Interface
3 : 8
Decoder
D23
3
4 : 16 Decode
4
22 Tasten
22 Keys S1-S22
12LEDs
Treiber
Driver
Treiber
Driver
D24/D25
8
7 Segment-An
7-segment dis
12 Latches

GA082